GaAs Power MESFET's: Design, Fabrication, and Performance

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Invited Paper

***Abstract*—This paper reviews the state of the art of power GaAs MESFET's. Items that will be covered are the operating principles of the device from a material and geometric point of view, the design, fabrication sequences, and material structures used by various laboratories, the factors identified as important to power by workers in the field, the performance of the device in terms of frequency effects, power per unit gate-width effects, scaling from small to large gate-width devices, and voltage effects. In addition, the circuit applications of GaAs FET's will be briefly discussed.**

I. INTRODUCTION

THE GaAs MESFET has been the "hottest topic" in the microwave device field over the last five years. Over 350 papers have been published on the subject since 1973, and five panel discussions at major conferences have been held over the last few years [1].

Why all this attention? Because the GaAs MESFET (FET) is a device with a broad range of applications. It is an outstanding low noise device from 2–40 GHz. It has been used as a mixer and as an oscillator. It is finding its way into IC's as a high speed switching element, and it is giving powers in the 4–20-GHz range never before reached by a transistor. So clearly, all the attention is justified!

The low noise and small signal properties of GaAs FET's have been the subject of most of the attention and also of review articles [2]–[6]. The power GaAs FET is a recent and exciting addition to the microwave device field. There have been recent articles dealing with power GaAs FET's [7]–[12], but to date a comprehensive review of the state of affairs of power GaAs MESFET's has not been made. This paper will attempt to give such a review.

The GaAs power FET is a relatively new but rapidly advancing device. In Fig. 1, the progress of power obtained from GaAs FET's at Bell Laboratories as a function of time is shown. Note that in a little over 2 1/2 years, powers have progressed from 0.5 to 18.5 W at 4 GHz. Bell Laboratories is not unique, and similar rapid advances have been made at Fujitsu, MSC, NEC, and Texas Instruments.

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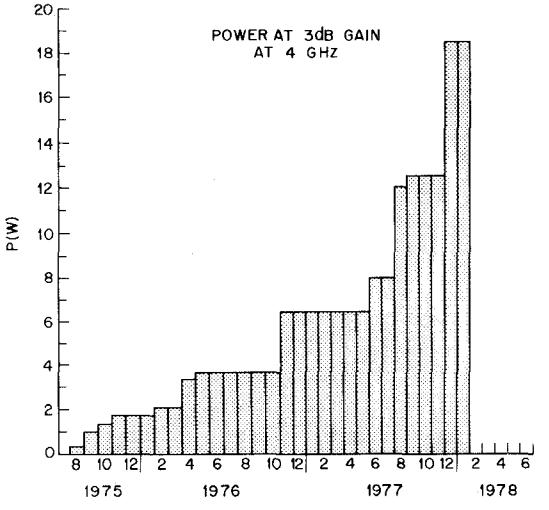

Fig. 1. Progress of power GaAs FET's at Bell Laboratories as a function of time.

The contents of this paper are as follows. In Section II, the operating principles of the device from a material and geometric point of view will be given. In Section III, the design, fabrication sequences, and material questions will be discussed. In Section IV, the microwave performance of the device will be discussed, including frequency and voltage effects. Section V includes our summary and conclusions.

II. OPERATING PRINCIPLES

The GaAs FET has received considerable attention from theoreticians. This work has fallen into the following general areas: a description of the device exclusively in terms of an equivalent circuit for a simplified intrinsic device with noise–current sources at the input and output for the purposes of calculating the noise properties of the devices [13]–[16], calculating the noise properties of the device from physical principles [17], or a calculation of the noise properties of the device from material and device parameters [18].

The power GaAs FET, on the other hand, has received little attention. Some efforts have been made to model the device in amplifier applications. For example, Hornbuckle and Kulhman [19] have used an equivalent circuit ap-

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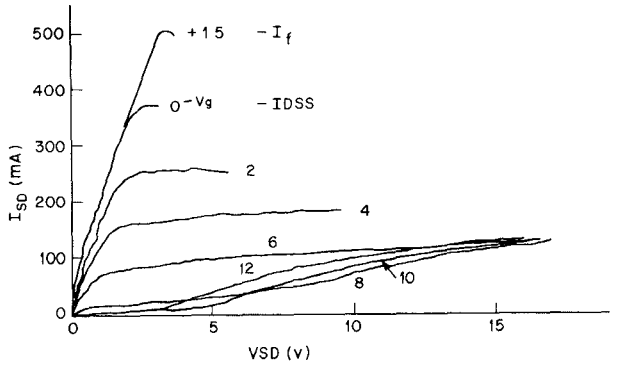

Fig. 2. $I-V$ characteristics of a 1-mm wide power GaAs FET.

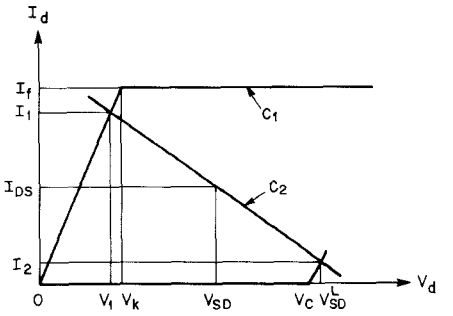

Fig. 3. Schematic representation of the $I-V$ characteristic of a power GaAs FET showing the important variables for power.

proach for designing medium power amplifiers, and Kotzebue [20] has taken a scattering parameter approach in the design of power amplifiers. Shur [21] and Shur and Eastman [22] have modeled the GaAs FET, postulating Gunn domain formation at the drain contact and calculating its effect on current saturation and breakdown voltage among other parameters. Very recently, Willing *et al.* [23] have addressed power performance of FET's by predicting large signal performance based on experimentally characterized bias dependence of device circuit model elements.

However, the actual channel properties that govern the power output of a GaAs FET have received little attention to date. To the designer of power GaAs FET's, the important design parameters are those which he can readily control in his fabrication process.

In Fig. 2, the $I-V$ characteristics of a power GaAs FET of 1-mm gate width is shown. This $I-V$ is displayed to indicate the important variables which influence a power GaAs FET.

If the operating frequency is below the current cutoff frequency of a GaAs MESFET, we can assume that the output power capability can be calculated based on its static drain characteristics. Reference to Fig. 2 shows two of the important static characteristics, namely the value of the saturated source–drain current I_{DSS}, the maximum drain current I_F, and the behavior of the drain current I_{SD} with gate voltage V_g and some drain potential V_{SD}. Note that at a V_{SD} equal to 9 V and $V_G \simeq$ to 8 V, significant curvature of I_{SD} versus V_{SD} is observed. Further increase in V_G results in increased rather than decreased I_{SD}. This behavior is expected for a classical FET device operating in a region of gate-to-drain avalanche.

In Fig. 3, a schematic of the $I-V$ characteristic shown in Fig. 2 is represented. This figure shows the drain current–voltage plane in which two curves are represented. Curve C_1 is a simplified representation of the maximum drain current I_F which is available with forward gate bias V_F (see Fig. 2).

Curve C_2 is the load line whose slope is the reciprocal of the load resistance R_L. Other parameters important in the understanding of the static characteristics are V_K, the knee voltage of curve C_1 and V_{SD}^L, the limiting source–drain voltage. To further understand what V_{SD}^L means, consider the following. The gate–drain avalanche breakdown voltage V_{GD}, for a gate biased to its pinch-off voltage V_P, limits V_{SD} by the following relationship:

$$V_{SD}^L = V_{GD} - V_p.$$

Beyond this point excess current appears in the drain circuit which cannot be modulated by the gate and, therefore, will not contribute to the output power of the device. For example, in Fig. 2, with 8 V on the gate and 8 V on the drain, the I_{SD} characteristics show avalanche. From the above relationship the V_{GD} would be calculated to be 16 V. This was in good agreement with the observed value of 16 V for the gate-to-drain breakdown.

From the current voltage characteristics and the parameters displayed in Fig. 2, a calculation of the output power can be made. If we assume that the dc bias point are V_{SD} and I_{SD}, and that the operation is harmonic at the bias point (V_{SD}, I_{SD}) for a current swing of $(I_1 - I_2)$, the output power available to the load would be

$$P_o = \frac{1}{8}(V_{SD}^L - V_1)(I_1 - I_2) = \frac{(V_{SD}^L - V_1)^2}{8R_L} = \frac{R_L}{8}(I_1 - I_2)^2$$

where

$$R_L = \frac{V_L^{SD} - V_1}{I_1 - I_2}.$$

These equations can be rewritten in terms of V_K, V_{GD}, and V_P to give the maximum output power P_m available from the device:

$$P_m = \frac{I_F}{8}(V_{GD} - V_P - V_K)$$

where

$$R_L = \frac{V_{GD} - V_P - V_K}{I_F}$$

$$V_{SD} = \frac{V_{GD} - V_P - V_K}{2}.$$

It can be seen, therefore, that the maximum output power P_m is given by the device parameters I_F, V_P, V_{GD}, and V_K. In practical terms let us consider a device with 350 mA/mm of I_F, a V_{GD} of 30 V, a V_P of 5 V, and V_K of 2 V which is not thermally limited. P_m is then

$$P_m = \frac{I_F}{8}(V_{GD} - V_P - V_K)$$

$$P_m = \frac{350\text{ mA}}{\text{mm } 8}(30\text{ V} - 5\text{ V} - 2\text{ V})$$

$$P_m = 1.0\text{ W/mm}.$$

Referring to Section IV, this calculation is in reasonable agreement with values obtained for output power/mm at 3–4-dB gain from power FET's.

The above derivations of output power are most accurate at large signal conditions under full RF swing. Thus agreement between calculated and experimental numbers at compressed conditions of 3–4-dB gain is to be expected. Under conditions of lower RF drive (see text in Section IV), the power/mm decreases, reflecting less of a current swing by the imposed sinusoidal signal on the gate. The calculation of the power, gain, and load resistance for power FET's in terms of device parameters operating over a wide range of RF drive conditions will be the subject of a forthcoming paper [24] and will not be presented here.

In summary then, the above discussions have pointed out that the important device parameters for power FET's are: I_F—the maximum drain current available with a forward biased gate V_F, V_K—the knee voltage at which I_F saturates, V_{GD}—the gate-to-drain avalanche voltage, V_P—the pinch-off voltage of the device, and V_{SD}^L—the limiting source–drain voltage at which the gate can no longer modulate the channel current.

In the design of power FET's there are obviously tradeoffs in the above parameters. For example, an increase in I_F by a doping increase affects V_{GD}. At a given doping an increase in I_F is accompanied by an increase in V_P. To date, a model is not available which can predict optima in channel design, and much of the optimization has been done using an empirical approach. Nevertheless, recognition of the important parameters mentioned above can lead to improved FET performance.

III. Device Structures

In surveying the various structures employed in the design and fabrication of power GaAs FET's, there are goals various laboratories have strived for. These can be summarized as: 1) to obtain the maximum gate width for the frequency of interest, 2) to minimize electrical parasitics, 3) to reduce thermal impedance, 4) to achieve a device capable of sustaining a high drain–source potential, and 5) to achieve a materials technology which gives consistent and reproducible effects.

A. Structures Used to Increase Gate Width

The approaches used to maximize gate width involve three separate designs at the present. A crossover structure has been utilized by Fujitsu [25], [26], and NEC [27] to maximize the gate width by paralleling. In Fig. 4, a photograph of a 13-mm wide device which Fujitsu has fabricated is shown. This device employs gate over source crossovers with SiO_2 as the dielectric. NEC's approach is similar. The main advantage of this approach is that it makes the most efficient use of real estate and minimizes the number of bonds required to assemble a large device. However, the processing is more complex, and additional parasitics are involved in the capacitance of the crossover. But Fujitsu has successfully fabricated a 26-mm wide device this way.

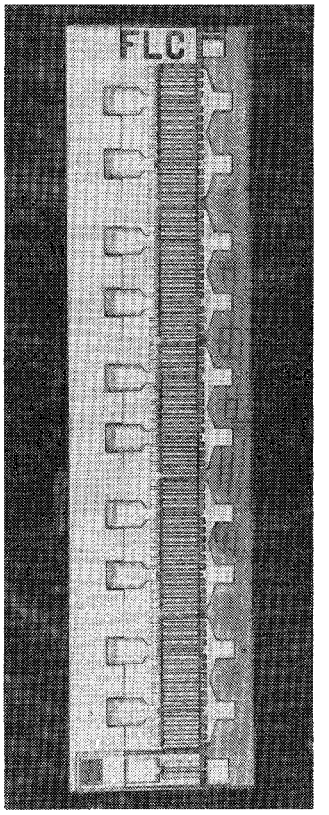

Fig. 4. Fujitsu FET (13-mm gate width).

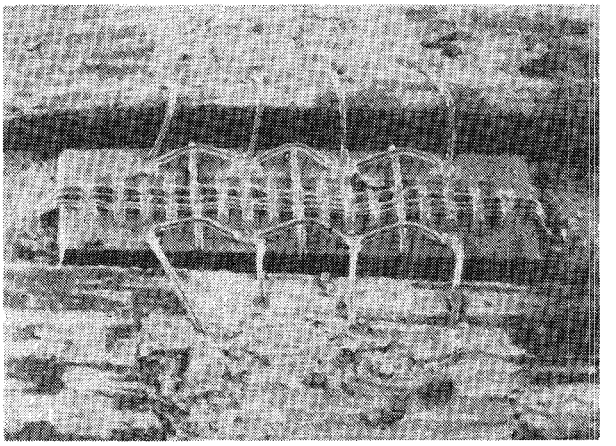

Fig. 5. Texas Instruments FET (4.8-mm gate width).

The second approach simply involved paralleling a large number of unit cells by wire bonding. Many laboratories have adopted this approach, examples of which are shown in Figs. 5 and 6. The device in Fig. 5, fabricated at Texas Instruments, has multiple source bonding pads and gate and drain buss bars. Devices as large as 9.6 mm for operation at 9 GHz [28] and 24 mm for operation at 4 GHz [29] (see Fig. 6) have been successfully assembled

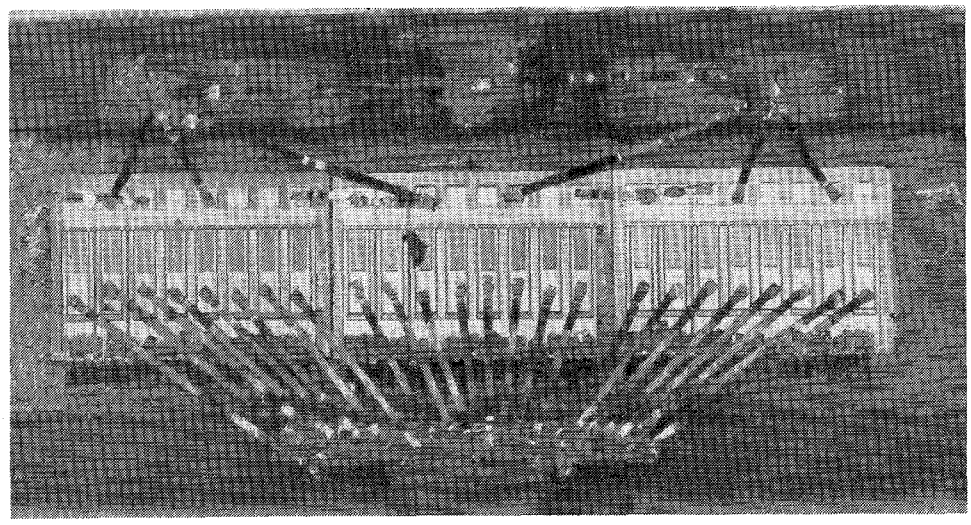

Fig. 6. Bell Laboratories FET (24-mm gate width).

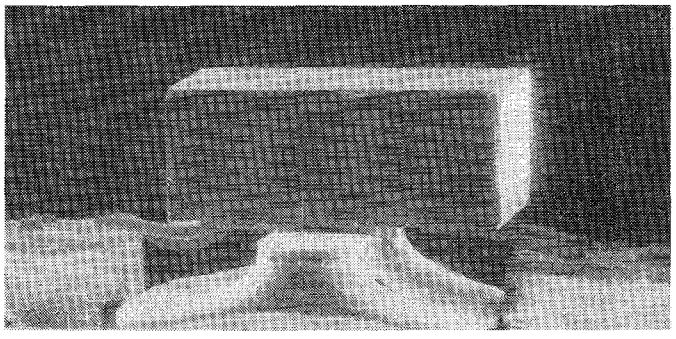

Fig. 7. MSC flip mounted FET (2.4-mm gate width).

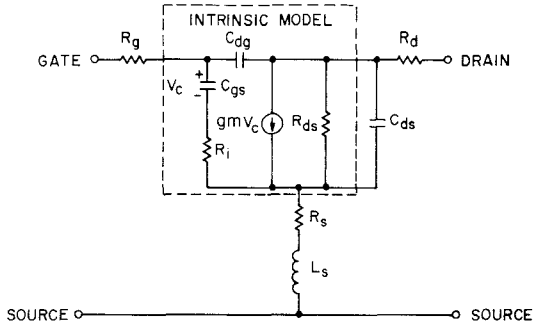

Fig. 8. Equivalent circuit for a GaAs power FET.

this way. The multiple bond approach allows a simple processing technology but makes device assembly more difficult and can have increased parasitics.

Another approach first introduced by RCA [30] and now used also by MSC [31] is shown in Fig. 7. This approach involves "flip chipping" plated up source pads to a package heat sink to achieve paralleling. While very large devices have not been made this way, in principle they could be.

B. Minimization of Parasitics

The effect of parasitics on FET performance can be understood by examining (1) which gives the maximum available small signal gain (MAG) calculated for the equivalent circuit of Fig. 8 [32], [33]:

$$\mathrm{MAG}=\left(\frac{f_T}{f}\right)^2\cdot\frac{1}{4g_{ds}(R_g+R_i+R_s+\pi f_T L_s)+4\pi f_T C_{dg}(2R_g+R_i+R_s+2\pi f_T L_s)} \tag{1}$$

and

$$f_T\approx\frac{g_m}{2\pi C_{gs}} \tag{2}$$

where

- f operating frequency,
- g_{ds} drain conductance,
- R_g gate series resistance,
- R_i channel resistance between source and gate,
- R_s source series resistance,
- L_S common source lead inductance,
- C_{dg} drain gate capacitance,
- C_{gs} gate source capacitance,
- g_m transconductance.

For given device parameters, MAG falls off 6-dB per octave increase in frequency. For this reason, minimization of electrical parasitic effects is particularly important to the design of FET's at the higher frequencies to prevent the gain from becoming unacceptably low. The fact that (1) applies to small signal operation does not negate the fact that factors important to optimization of small signal devices apply to power devices as well since high power is not useful with very low gain. For example, in order to obtain significant output power at reasonable gain levels at X-band and higher frequencies, it has been found that gate lengths of 1 μm or less are required [28], [34]. Shorter gates lead to increased values for f_T (2) since g_m increases and C_{gs} decreases with decreasing gate length.

TABLE I
EFFECT OF SOURCE LEAD INDUCTANCE ON MICROWAVE PERFORMANCE

	Gain (db)	# Cells	P_{out} (W)	η_{PA} (%)	V_{DS} (V)	Combining Efficiency (%)
One Chip	4	1	0.91	25.6	8	79.1
		4	2.88	24.1	8	
	6	1	0.83	31.8	8	
		4	2.14	19.9	8	64.5
Four Chips	4	1	0.96	39.3	8	96.9
		4	3.72	36.8	8	
	6	1	0.87	45.3	8	97.4
		4	3.39	40.0	8	

Many parasitic effects must be considered in power FET design. The most significant parasitic effect that must be considered results from the source lead inductance L_S that appears in (1). Minimization of this parameter is far more difficult for power FET's than small signal devices. Most power FET designs involve combination of several cells with each cell having several parallel gate fingers. The cells must be combined in some manner, either integrated on the chip during processing or during the bonding operation. In principle, cells can be added until the impedance becomes too low for it to be matched in the microwave circuits. If the source lead inductance (and resistance) can be neglected, then the quantities appearing in (1) scale in such a way that the MAG is unchanged. The effect of source lead inductance on cell combination is illustrated schematically in Fig. 8. Unless special care is taken, the MAG will be degraded when cells are combined because the source lead inductance is not reduced proportionally as cells are added.

A four-cell Texas Instruments device mounted in a test circuit was shown in Fig. 5. The microwave performance of four cells connected in this manner can be compared with the performance of a single cell by calculating the cell combining efficiency [34]. Table I compares the output power from one and four cells at both 4- and 6-dB gain. The cell combining efficiency is defined as

$$\eta = \left.\frac{P_{\text{out}}(4 \text{ cells})}{4P_{\text{out}}(1 \text{ cell})}\right|_{\text{constant gain}} \tag{3}$$

and is given in the table.

To determine the effect of reduced source lead inductance on combining efficiency, four single-cell chips were mounted side by side with the sources independently grounded. The significant improvement in combining efficiency shown in Table I is attributed to reduced source lead inductance.

Fig. 9 shows a new plated heat sink power FET configuration now under development at Texas Instruments [34]. This structure reduces the source inductance by allowing source grounding between cells without the need for using separate chips. The thermal advantages of this structure are discussed in the next subsection.

D'Asaro *et al.* [35] of Bell Laboratories have taken a somewhat different approach to reducing source lead inductance. Fig. 10 shows the cross section and cell layout of an FET with low inductance via connections through the substrate. This device has a plated heat sink. Fig. 11 compares the microwave performance of devices fabricated with the substrate via connection with conventional devices of the same type. There is a significant increase in gain (1–2 dB) for output powers 2 dB or more below saturation. The saturated output power is unchanged.

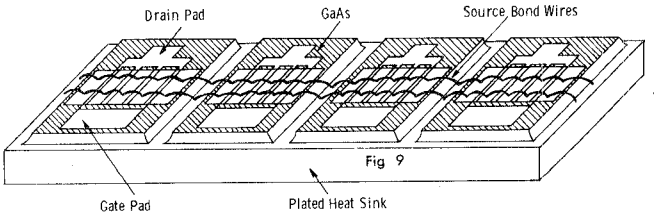

Fig. 9. Texas Instruments plated heat sink FET.

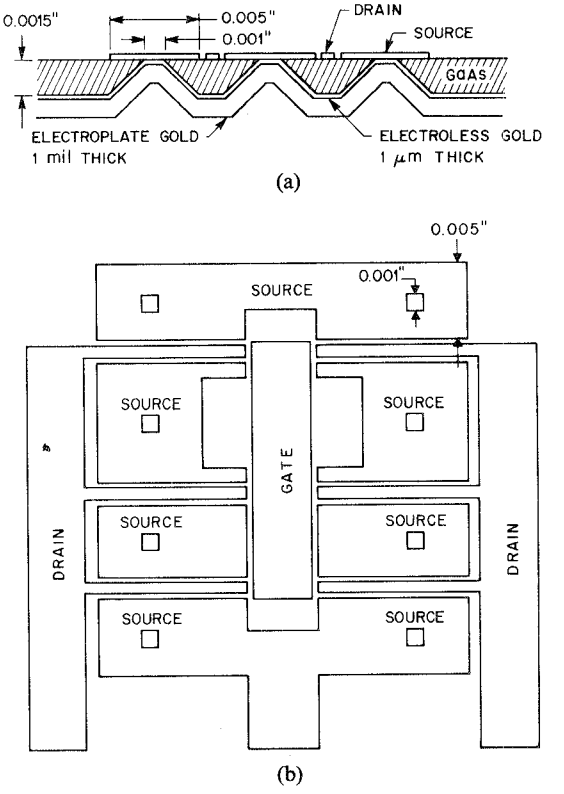

Fig. 10. Bell Laboratories via FET. (a) Cross section. (b) Top view.

There have been several other approaches to minimization of source lead inductance in the development of GaAs power FET's. One of the most promising is flip chip mounting as was mentioned earlier and shown in Fig. 7. This approach is not widely used because of the difficulty in implementation.

It is not obvious which of the approaches for reducing the source lead inductance is optimum. Each has its advantages and disadvantages, particularly in ease of implementation. As power FET performance is pushed to higher and higher frequencies, reduction of source lead inductance becomes more and more important due to the

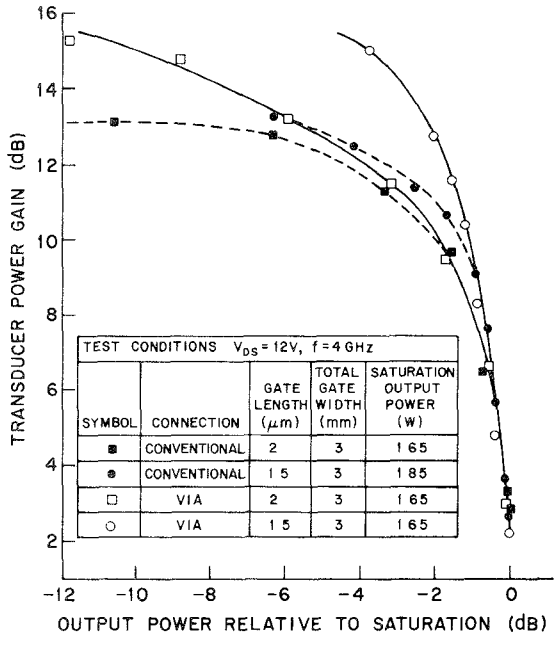

Fig. 11. Microwave performance of the via FET compared with a conventional FET.

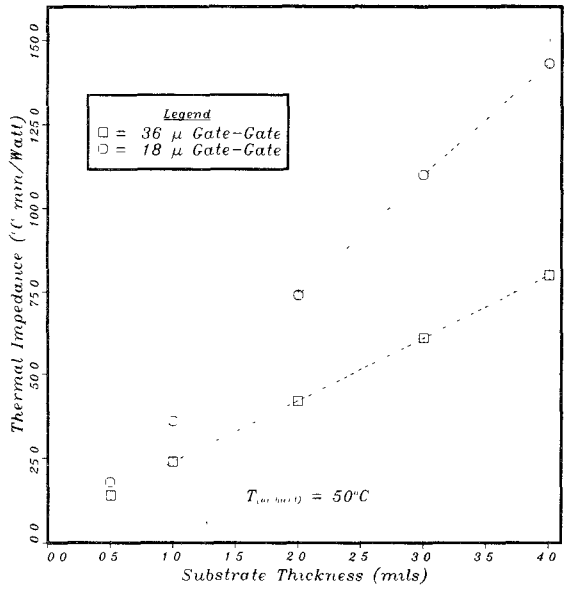

Fig. 12. Thermal comparison of power FET's.

expected gain rolloff with frequency. Further effort in this area is anticipated.

There are other electrical parasitic effects that may be important for power FET's. Fukuta *et al.* have treated the gate finger as a transmission line and have determined the phase and amplitude changes of the input signal as a function of position along the gate [33]. Their results indicate that gate finger widths should be 100 μm or less, even at 4 GHz; however, Macksey has experimentally examined the effect of gate finger width on microwave performance and determined that degradation at 10 GHz does not begin until finger widths of 200 μm are reached [36]. Finger widths of 500 μm at 4 GHz [37] and 75 μm at 18 GHz [34] have been used successfully, but *Ku*-band performance has not been optimized at this time.

A design consideration that has received little attention at this point is the phase relationship between the signals at different cells or at different fingers along a large cell. Improper phasing could lead to less than optimum combining of large transistors. This is an example of the conflict between electrical and thermal design parameters. Chip size should be minimized from electrical design considerations. Maximum distance between gate fingers and, hence, maximum chip size is desirable from a thermal point of view. This will be discussed in more detail below.

C. Reduction of Thermal Impedance

Careful consideration must be given to the thermal design of power FET's if their microwave performance is to be optimized. At the present time, power FET's with widely differing configurations are under development at a number of laboratories. Since the thermal analysis of these devices depends greatly on the details of device geometry and requires solution of a three-dimensional heat flow problem, it is difficult to compare the various approaches. However, the two parameters which demonstrate thermal design are the substrate thickness and gate-to-gate separation.

Most power FET's currently being developed are mounted upright on the heat sink so that the heat must be removed through the GaAs substrate. Solutions of this thermal problem have been carried out for different device geometries by Wemple and Seman [38]. In Fig. 12 the maximum temperature rise under the gate as a function of substrate thickness and gate-to-gate spacing is shown. This calculation takes into account the temperature dependence of the thermal conductivity of GaAs. It is obvious that the substrate thickness plays a major role in determining the temperature rise. But of great importance and of equal effect for substrate thicknesses of two or more mils, is the gate-to-gate spacing. The plated heat sink FET's described in the preceding sections and illustrated in Figs. 9 and 10 permit handling of the FET after the substrate thickness is reduced [34], [35].

Huang *et al.* [39] have calculated the thermal resistance of flip chip mounted power FET's of the type developed at RCA and MSC and shown in Fig. 7. In this case, the heat is removed through the Au source pads. The heat must spread into the GaAs, and this spreading resistance is again the dominant factor in the thermal resistance. There is an additional spreading contribution from the Au source pad into the heat sink that cannot be neglected.

As was stated above, the advantages of one FET configuration over another are highly dependent on the details of the device geometry and mounting configuration. For thick GaAs substrates, flip chip mounting can have a thermal advantage. By going to thin substrates (refer to Fig. 12), upright FET's can have a thermal advantage

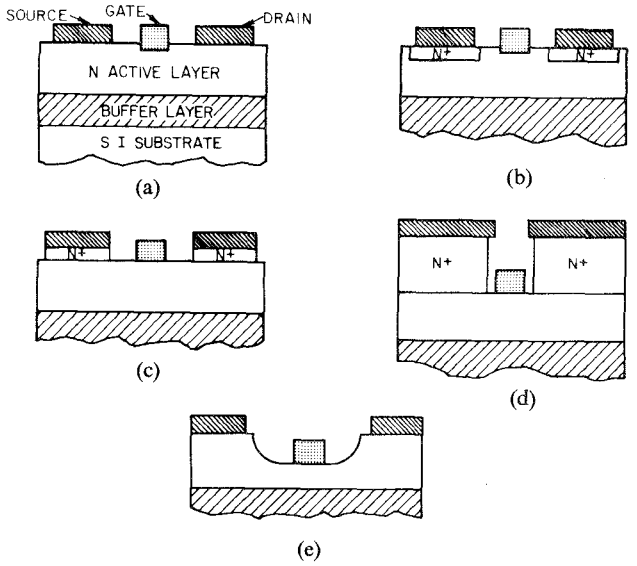

Fig. 13. Schematic of various FET structures. (a) Planar alloyed contacts. (b) Inlaid N^+ contacts. (c) Planar N^+ contacts. (d) Recessed channel with N^+ contacts and self-aligned gate. (e) Recessed channel.

because of the spreading resistance contribution from the source pads on flip mounted devices. The calculations of Wemple and Seman indicate that a substrate thickness of 50 μm gives the same thermal resistance as an equivalent flip-mounted device. In both cases, the size of the source pads and separation of the gate fingers is important.

Two techniques are commonly used to make thermal resistance measurements, the infrared scanning microscope and a temperature sensitive neumatic liquid crystal [40]. The resolution possible with the latter is $\sim$5 μm compared with 25–50 μm for the infrared microscope. Higher values for the thermal resistance are obtained using the liquid crystal technique which is probably more accurate.

Recently, the thermal resistances of plated heat sink FET's were measured [34], [38]. The results confirm the theoretical calculation. For example, for a 2-mil thick substrate, and a gate-to-gate spacing of 36 μm for a device dissipating $\approx$1 W/mm, a thermal impedance of 30°C mm/W was measured using the liquid crystal technique. There are limits to the use of thinner substrates, however, since the thickness cannot be reduced beyond the point where the increase in electrical parasitics leads to degraded microwave performance.

D. Structures Designed to Improve Source–Drain Burnout

In Fig. 13 a schematic of various structures is shown as a point of reference for the following discussions. The role of ohmic contacts in the drain–source burnout is now clearly established. In 1976, Wemple and Niehaus [41] demonstrated that avalanche at "imperfect" drain ohmic contacts (see Fig. 13(a)) triggers thermal runaway in the substrate and suggested the N^+ epi under the contacts (see Fig. 13(b)) would improve device voltage capability. Fujitsu first demonstrated this effect, and shortly thereafter the effect was verified by Niehaus *et al.* [37]. In Table II, a summary of contact technologies designed to increase the source–drain burnout voltage is listed for laboratories which have published on this question.

TABLE II

LABORATORY	TECHNOLOGY	OHMIC CONTACT	INSTANTANEOUS
Fujitsu	N^+ inlaid source and drain islands formed by selective epitaxial regrowth, epi channel	AuGe	Burn-out voltages >26V at 100 ma/mm
NEC	Recessed channel, no N^+ epi, epi channel	AuGe/Ni	Up to 22-25V at 100 ma/mm
H-P	N^+ inlaid source and drain islands formed by ion implantation, channel formed by island implantation	NiCr/Ge/Au	>30V at 100 ma/mm
BTL	N^+ epi planar source and drain contacts, epi channel	AuGe/Ag/Au	Up to 52V at 100 ma/mm

Fujitsu's approach has involved the formation of *inlaid* N^+ regions into the channel as shown in Fig. 13(b). Fujitsu is presently growing the inlaid N^+ regions by selective epitaxy. A similar design approach involving inlaid N^+ regions is used by Hewlett–Packard (see Table II) [42]. *However*, Hewlett–Packard utilizes ion implantation to form both the N^+ source and drain regions as well as the active channel.

Another approach involving N^+ contacts under the source and drain which might be termed planar contacts are used by Bell Laboratories among others (see Fig. 13(c)). In this design approach, epitaxy is used to grow the N^+ layer over the active N channel and then the N^+ is removed selectively in the region between the source and the drain to form the gate.

An extension of this technology involves the use of very thick N^+ regions under the source and drain, and a fabrication sequence which utilizes an overhanging source and drain electrode to produce a self-aligned gate (see Fig. 13(d)). This approach was started by RCA [30] and is now used by MSC [31].

Finally, NEC [43] has recently introduced a structure termed the recessed contact structure (see Fig. 13(e)), which they have demonstrated increases the burnout voltage in their power FET's. NECs contention is that N^+ contacts are not required to achieve high source–drain burnout, and by reducing the field at the drain contact, which their structure does, high voltages are achieved.

In Table II, the values of the instantaneous burnout voltages for the various structures listed are given. In an attempt to normalize results from different laboratories, we have cited the burnout voltages at 100 mA/mm of drain–source current. Values as high as 52 V have been achieved, but it is dangerous to conclude that the planar N^+ epi contacts are the best since each laboratory has channels which differ widely in doping, pinch-off voltage, source–drain spacings, etc. In fact, NEC [43] has recently

compared structures 1, 2, 3, and 5 in Fig. 13 and concludes that there is very little difference in the burnout voltage between these structures.

E. Materials for Power GaAs FET's

The material requirements for FET's are quite stringent. Uniform thin epitaxial films with thicknesses of approximately 0.2–0.6 μm are necessary. In addition, it is now clear that buffer layers improve the performance of devices in general and N^+ layers under ohmic contacts improve the characteristics of the devices as well as the contacts. Therefore, one can summarize by saying that a materials technology for FET's should be capable of growing multilayer, thin uniform epitaxial structures with a wide range of doping variations, typically 10^{13}–10^{18} cm^{-3}. In addition, abrupt transitions between the different layers are required, and surface smoothness is a prerequisite for device processing.

The materials technology most widely used for producing FET structures is CVD. MBE and LPE are used but have not gained widespread use. Recently, ion implantation has demonstrated promise as a technique for producing material, but most of the results have been on low noise devices [44], and this technique will not be discussed further here.

Buffer layers have been a subject of much research over the last few years. Nozaki *et al.* [45] first showed that the introduction of buffer layer increases the mobility of electrons in the active layer near the pinch-off point. This result has been verified by many workers. However, the growth of buffer layers on semi-insulating substrates is a complicated process. Cox and DiLorenzo [46] have shown that the typical "undoped" buffer layer used by many workers in the field is actually a layer compensated by the diffusion of acceptors from the semi-insulating substrate. Depending on growth conditions, the transition to the active layer may be in a region of heavy compensation. However, if the buffer layer is grown too thick, a conductivity region may develop under the active layer [46].

In order to eliminate some of the problems of undoped buffer layers, various laboratories have attempted to introduce chromium or iron during the growth of the layer. It was shown that chromium can be introduced using $Cr_2O_2Cl_2$ [47] in CVD resulting in epitaxial layers with resistivities of 10^8 $\Omega\cdot$cm. Iron was also used [48] as a dopant by transport with HCl, but resistivities only as high as 10^5 $\Omega\cdot$cm were obtained. To date, a systematic study of the difference between compensated undoped buffer layers or chromium or iron dopant buffer layers has not been made.

With the success of N^+ layers under ohmic contacts, it is of interest to see what materials technologies are being used to grow these layers. Fujitsu's approach [25] has been to use an organometallic CVD system to grow selective inlaid N^+ regions through an SiO_2 mask. Their approach, while complicated, has met with success. The more straightforward technology is simply to grow an N^+ layer [37], [46] over the active layer using a dopant such as sulphur or silicon to obtain doping levels of $2\text{–}3\times10^{+18}$ cm^{-3}. And, finally, ion implantation has been used [42] to selectively produce regions of high doping under ohmic contacts.

The direction for future materials work appears to be concentrated in four areas. The buffer layer question will continue to receive attention, and further optimization is expected. Ion implantation looks like a promising future technology. CVD improvements are expected in the area of low temperature CVD [49] growth, graded doping profiles [50], and the use of organometallic systems. Finally, MBE [51] is expected to make an impact in the near future.

IV. Microwave Performance

A. Device Results and Frequency Dependence

In Table III, a summary of microwave results obtained from various laboratories is listed. The data are obtained primarily from private communications from the listed laboratories, although some of the results have been published. Some points worthy of note from Table III are as follows. Powers up to 18.5 W have been obtained at Bell Laboratories at 4 GHz but with significant gain compression. Approximately 11 W with 8-dB gain or 15 W with 5-dB gain have been obtained at 4 GHz. Powers as high as 4.2 W at 10 GHz with 4.3-dB gain and 0.85 W at 18 GHz with 4.0-dB gain have been obtained at Texas Instruments. Note one very interesting point: if we define a figure of merit for the device as power/width or W/mm at 3–4-dB gain, then up to 1 W/mm can be obtained at frequencies as high as 16 GHz, suggesting very little frequency dependence of power/width at 3–4-dB gain. This is expressed graphically in Fig. 14 where we have plotted the best power/width as a function of frequency at 3–4-dB gain and compare it to a $P\sim f^{-2}$ dependence.

In Fig. 15 the power output dependence on frequency is plotted where it is clearly shown that the power dependence is

$$P_{\text{out}} f^2 \cong \text{constant}.$$

B. Power and Gain Scaling

1) Frequency Dependence: In Fig. 16, the maximum width for scaling, $W_{\max}$(mm), is plotted as a function of frequency. The data points were obtained by surveying published or privately communicated results by asking up to what width does the power scale to within 30 percent of a very small device with similar characteristics from the same laboratory. For example, the data point at 16 mm at 4 GHz was obtained from a Bell Laboratories result [52] which showed 0.84 W/mm at 16-mm width compared to 1.05 W/mm at 4-mm at 4 GHz.

The data presented in Figs. 14 and 15 suggest that the frequency performance of power GaAs FET's at present is limited by the ability to either match or uniformly feed large transistors as the frequency increases. This situation

TABLE III
GaAs Power FET Microwave Performance

f (GHz)	P_{out} (W)	Gain (dB)	W (mm)	P_{out}/W (W/mm)	Laboratory
4	15.0	5.0	26	0.58	Fujitsu
	9.6	5.0	13	0.74	
	18.5	3.5	24	0.77	Bell Labs
	14.4	3.5	16	0.90	
	10.7	8.1	16	0.67	
	3.6	3.0	3	1.2	
	3.0	4.7	9.6	0.31	RCA
6	6.5	4.0	22.4	0.29	NEC
8	5.1	5.0	6.4	0.80	TI
	3.9	7.0	4.8	0.80	
	1.7	4.0	1.2	1.42	
	2.2	4.2	5.2	0.42	Fujitsu
	1.1	4.0	1.0	1.1	Bell Labs
	63	7.7	1.0	63	
10	4.2	4.3	6.4	0.65	TI
	3.9	6.0	4.8	0.80	
	1.2	5.3	2.4	0.50	RCA
	1.2	4.0	2.8	0.43	Westinghouse
12	2.10	4.0	3.6	0.58	TI
14	0.6	4.0	3.0	0.20	NEC
16	1.10	4.0	1.2	0.92	TI
18	0.85	4.0	1.2	0.71	TI
22	0.14	4.8	0.6	0.23	RCA

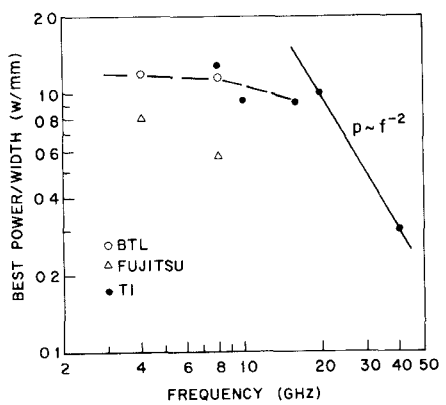

Fig. 14. Best power/width (W/mm) at 3–4-dB gain as a function of frequency.

is true under conditions where gain is on the order of 3–4 dB and the transistor is operated with significant gain compression. The performance of the transistor at smaller signal operation in the vicinity of 6–12-dB gain is more complex. A systematic study of dependence of power on frequency at smaller signal operation has not been done. However, some trends are evident. For example, results from Bell Laboratories [53], [54] comparing a 1.0-μm gate length, 1-mm gate-width device with 4250-μm gates showed the following.

	4 GHz	6 GHz	8 GHz
Gain at≈100 mW of RF input	9.1 dB	8.1 dB	7.7 dB

This result means that GaAs FET's operated as power devices do not show a 6-dB/octave gain reduction typical

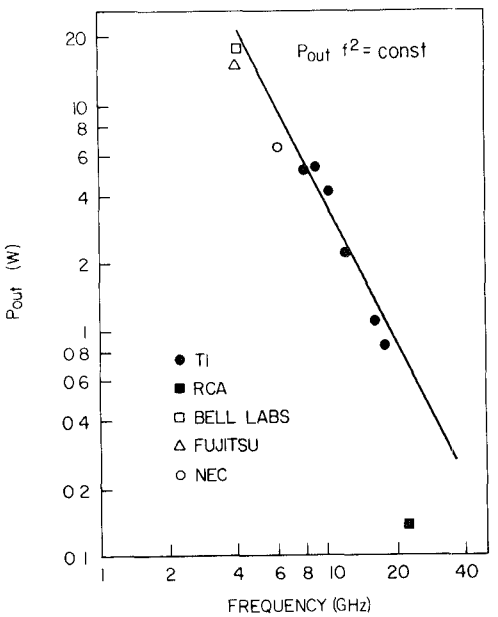

Fig. 15. Power output dependence on frequency.

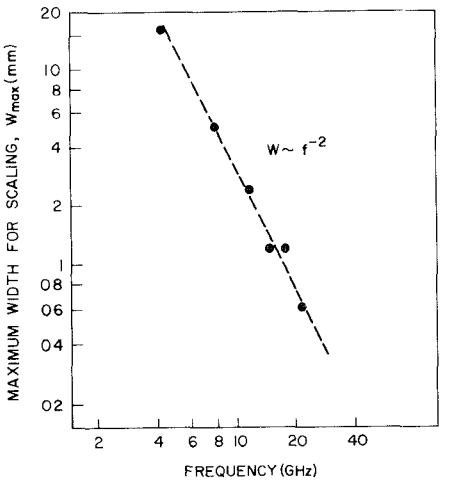

Fig. 16. Maximum width for scaling W_{max} (mm) as a function of frequency.

TABLE IV
Scaling Performance in Power FET's with Size

Size (MM)	(W/mm at 3 dB Gain)
1.0	1.3
3.0	1.3
8.0	0.90
16.0	0.90
24.0	0.77

of that deduced from small signal properties such as S parameters. Secondly, the gate length plays an important role as the device is operated in a smaller signal regime. For example [29], at 4 GHz, a 1-mm wide submicrometer gate-length device gave 17-dB gain with approximately 0.1 W out and 13–14-dB gain with approximately 0.5 W out. Both of these devices gave about 1.1 W out at 4-dB gain.

2) Size Dependence at a Given Frequency: In Table IV, the performance of devices fabricated at Bell Laboratories ranging in size from 1.0 to 16 mm is shown. The table lists

TABLE V
SCALING PERFORMANCE AT 24-V SOURCE–DRAIN BIAS

Size	3 dB power	3 dB power/mm	Gain at 106 mW/mm input	Output power at this gain
mm	W	W/mm	dB	W
4	4.2	1.05	9.4	3.6
6	5.4	0.9	8.7	4.7
8	7.2	0.9	8.6	6.2
16	13.5	0.84	8.1	10.7

the output of the device in W/mm at 3-dB gain at 4 GHz. Note that between 1.0–3.0 mm there is no loss of power. At 8-mm width, the power/width has decreased to 0.90 W/mm which remains constant up to 16 mm. The power/width has decreased to 0.77 W/mm at 24 mm. The data in Table IV are on devices from different slices, and the results are somewhat difficult to interpret but indicate clearly a loss in performance as the size is increased.

Wemple *et al.* [52] have done a detailed study of the effect of size on performance at 4 GHz within the same slice. These data are shown in Table V, where the power/mm, gain at 106-mW/mm input and output power at that gain are shown. The degradation from 4 to 16 mm is 1.3 dB in gain at a fixed input (106 mW/mm) but less in 3-dB power where 1.0-dB degradation is observed. Macksey *et al.* [34], [40] have shown a similar dependence on size in smaller devices operating at *X*-band.

A detailed explanation has not been given for the loss, but it would appear that the inability to uniformly feed larger transistors and circuit losses due to low device impedance are two main contributing factors.

The Texas Instruments results [34] indicate that source lead inductance is a major factor in accounting for the lower power/width obtained for large devices compared with smaller ones. Table I showed how the cell combining efficiency (and hence power/width) is increased by reducing the source lead inductance.

C. Dependence of Microwave Performance on Source–Drain Voltage

In Fig. 17, the dependence of the power and gain at a fixed input power and the power at fixed 3-dB gain is plotted as a function of source–drain voltage [52]. This device had an I_{DSS} of 150 mA/mm, pinch-off voltage of 4.5 V, and an active layer doping of 5×10^{16} cm^{-3}. The value of the gate-to-drain avalanche measured as a diode was ~25 V. The burnout voltage of this device was greater than 35 V. Up to 16 V_{SD}, the power and gain increases almost linearly, and above that significant curvature is seen. The interpretation of Wemple *et al.* [52] for this curvature is that the 25-V breakdown of the gate is exceeded during RF operation at drain voltages of ~15 V, and at drain voltages higher than this the avalanche component of the I–V characteristic reduces the power substantially as was pointed out in Section III.

Macksey *et al.* [40] have studied the effect of temperature on the performance of GaAs FET's and concluded that the saturation effect of power with V_{SD} is due principally to thermal effects. However, the Macksey *et al.* device had a 4-mil thick substrate, and the Wemple *et al.* device had a 1.5-mil thick substrate. As pointed out in Section III, the thermal impedance of the device is very substrate-dependent, and one would expect that the 4-mil thick device would be limited more severely by temperature use.

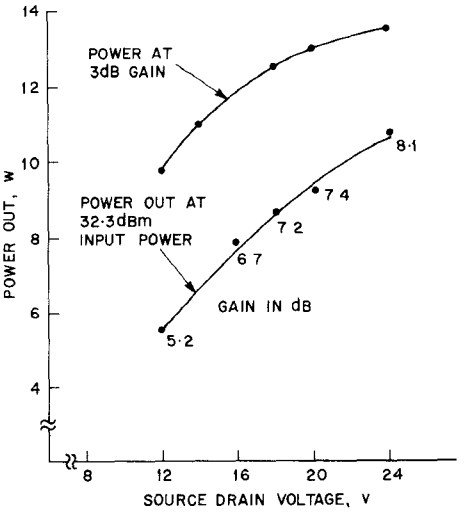

Fig. 17. Power and gain at fixed 32.3-dB input power (106 mW/mm) and power at a fixed decibel gain as a function of source–drain bias for a 16-mm device.

The above two results indicate that both thermal and avalanche effects are important in limiting the output power of GaAs FET's as the source–drain bias is increased. But it is clear that by proper optimization of the channel for improved avalanche and of the thermal impedance of the device, significant improvements in performance are available with higher V_{SD}. In addition, the amplifier designer receives a benefit of easier matching to the device operated at high V_{SD}.

V. SUMMARY AND CONCLUSIONS

The microwave performance of GaAs power FET's has improved rapidly over the past several years as a result of efforts at several laboratories. Output ranging from 18.5 W at 4 GHz to 850 mW at 18 GHz have been achieved. While the maximum output powers obtained to date follow the $P\sim f^{-2}$ dependence typical of solid-state microwave devices, the power/width figure of merit described in Section IV for small structures is nearly independent of frequency with a value of approximately 1 W/mm. With a constant power/width ratio, the maximum that can be obtained at a given frequency is determined by the total gate width that can be used without performance degradation.

We have reviewed in this paper the design approaches that are being used to optimize power FET performance. While the approaches differ in a number of ways, they all directed at maximizing the power/width ratio while utilizing the maximum total gate width. The power/width ratio can be increased by reducing the device thermal imped-

ance, by increasing the drain–source breakdown voltage (and the operating voltage), by optimizing material parameters at a given frequency (doping level, layer thickness), and by optimizing the device geometric factors (e.g., gate finger width). The maximum total gate width can be increased by reducing electrical parasitics, particularly the source lead inductance. Since many of the design factors mentioned above are not independent of each other, a variety of device designs have evolved that depend, to some extent, on the frequency of interest.

Further advances in power FET performance are anticipated. In light of the recently reported operation of low noise FET's at 30 GHz [55], power FET's operating at that frequency can be expected in the near future. Performance improvements will be seen at all frequencies with output powers of up to 10 W likely at X-band and corresponding increases ($\sim f^2$) being achieved at other frequencies until thermal limitations dominate at the lower frequencies.

Although the limits of power FET performance have not been reached, present performance levels are sufficiently high to have created widespread interest in systems applications of these devices. For example, Schroeder and Gewartowski [56] recently reported on a 2-W 4-GHz amplifier that is expected to have a wide application in radio relay systems. Tserng and Macksey [57] have developed a 4-W 10-GHz amplifier module that is suitable for phased array radar applications provided that significant cost reductions can be achieved. Power combining techniques are being developed [58] that will result in replacement of TWT's by FET amplifiers in many system applications.

Future work on the development of power FET's must include increased emphasis on device reliability. While some aspects of the reliability studies that have been conducted on low noise FET's [59] apply to power FET's as well, the effect of the higher operating temperatures and dc and RF electric fields that power FET's must withstand will require additional tests. It is known that tests are underway at some laboratories; however, no results of a comprehensive study have been reported at this time.

In conclusion, the authors feel that the future for GaAs power FET's is bright. Advances in performance will continue at a rapid pace but some emphasis will shift to reliability studies and to the establishment of low-cost fabrication procedures in order to increase acceptance of these devices in systems application.

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